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| Issue | December 21, 2024 |
| Rev. | 1.0 |
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CRYSTAL UNIT SPECIFICATIONS

客户批准 Customer Approval

(请批准后回签一份 **Please Return A Copy With Approval**)

| | |
|----------------------|----------------------------------|
| Customer | |
| Customer P/N | |
| Product | SMD 5032 XO |
| Spec | POSC5032J/19.44M~320.000M |
| A-Crystal P/N | AOC Series |

| | | |
|--------------------|-----------------|-----------------|
| Drawn | Checked | Approved |
| <i>Caoqiaobang</i> | <i>Fengying</i> | <i>Tanqlong</i> |



1. ELECTRICAL SPECIFICATIONS

1.1 Hold Type: POSC5032J

| No. | Item | Symb | Electrical Specification | | | | Remark |
|-----|-----------------------------|-----------|-----------------------------------|------|-----------|--------------------|------------------------------|
| | | | Min. | Type | Max. | Units | |
| 1 | Nominal Frequency | F_0 | 25.00 | | 250.00 | MHz | |
| 2 | Frequency Stability | ST | ± 25 | | ± 100 | ppm | |
| 3 | Operating Temperature Range | T_{OPR} | -20 | | +125 | $^{\circ}\text{C}$ | |
| 4 | Storage Temperature Range | T_{STG} | -55 | | +125 | $^{\circ}\text{C}$ | |
| 5 | Power supply Voltage | V_{DD} | 2.5 | | 3.3 | V | $\pm 5\%$ |
| 6 | Start UP Time | T_{OSC} | | | 10 | ms | To 90% of Final Amplitude |
| 7 | Output waveform | | LVDS Electrical Characteristics | | | | |
| 8 | Current Consumption | I_{CC} | | | 60 | mA | $R_L=50\Omega$ to VDD -2V |
| 9 | Standby current | I_{CC} | | | 30 | μA | OE=LOW |
| 10 | Output Voltage High | V_{OH} | | 1.43 | 1.6 | V | |
| 11 | Output Voltage Low | V_{OL} | 0.9 | 1.1 | | V | |
| 12 | Rise Time | T_r | 0.5 | | 1.0 | ns | 20% ~ 80% Output Swing |
| 13 | Time Fall | T_f | 0.5 | | 1.0 | ns | 80% ~ 20% Output Swing |
| 14 | Symmetry | TH/T | 45 | 50 | 55 | % | |
| 15 | Enable Voltage High | | 0.7VDD | | | v | Note 2, (Logic 1) |
| 16 | Enable Voltage Low | | | | 0.3VDD | v | Note 2, (Logic 0) |
| 17 | Output Enable Delay Time | | | | 2 | ms | |
| 18 | Output Disable Delay Time | | | | 200 | ns | |
| 19 | Output waveform | | LVPECL Electrical Characteristics | | | | |
| 20 | Current Consumption | I_{CC} | | | 80 | mA | $R_L=50\Omega$ to VDD -2V |
| 21 | Standby current | I_{CC} | | | 10 | μA | OE=LOW |
| 22 | Output Voltage High | V_{OH} | VDD-1.025 | | VDD-0.88 | V | |
| 23 | Output Voltage Low | V_{OL} | VDD-1.81 | | VDD-1.62 | V | |



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ELECTRONIC TECHNOLOGY CO., LTD.



| | | | | | | | |
|----|---------------------------|---------------------------------|--------|-----|--------|----|------------------------|
| 24 | Rise Time | Tr | 0.5 | | 1.0 | ns | 20% ~ 80% Output Swing |
| 25 | Time Fall | Tf | 0.5 | | 1.0 | ns | 80% ~ 20% Output Swing |
| 26 | Symmetry | TH/T | 45 | 50 | 55 | % | |
| 27 | Enable Voltage High | | 0.7VDD | | | v | Note 2, (Logic 1) |
| 28 | Enable Voltage Low | | | | 0.3VDD | v | Note 2, (Logic 0) |
| 29 | Output Enable Delay Time | | | | 2 | ms | |
| 30 | Output Disable Delay Time | | | | 200 | ns | |
| 31 | Output waveform | HCSL Electrical Characteristics | | | | | |
| 32 | Current Consumption | I _{CC} | | | 40 | mA | RL=50Ω to VDD -2V |
| 33 | Standby current | I _{CC} | | | 10 | uA | OE=LOW |
| 34 | Output Voltage High | V _{OH} | 660 | 740 | 850 | mV | |
| 35 | Output Voltage Low | V _{OL} | -150 | 0 | 150 | mV | |
| 36 | Rise Time | Tr | 0.5 | | 1.0 | ns | 20% ~ 80% Output Swing |
| 37 | Time Fall | Tf | 0.5 | | 1.0 | ns | 80% ~ 20% Output Swing |
| 38 | Symmetry | TH/T | 45 | 50 | 55 | % | |
| 39 | Enable Voltage High | | 0.7VDD | | | v | Note 2, (Logic 1) |
| 40 | Enable Voltage Low | | | | 0.3VDD | v | Note 2, (Logic 0) |
| 41 | Output Enable Delay Time | | | | 2 | ms | |
| 42 | Output Disable Delay Time | | | | 200 | ns | |
| 43 | Package type | 5.0*3.2*1.4 | | | | | |

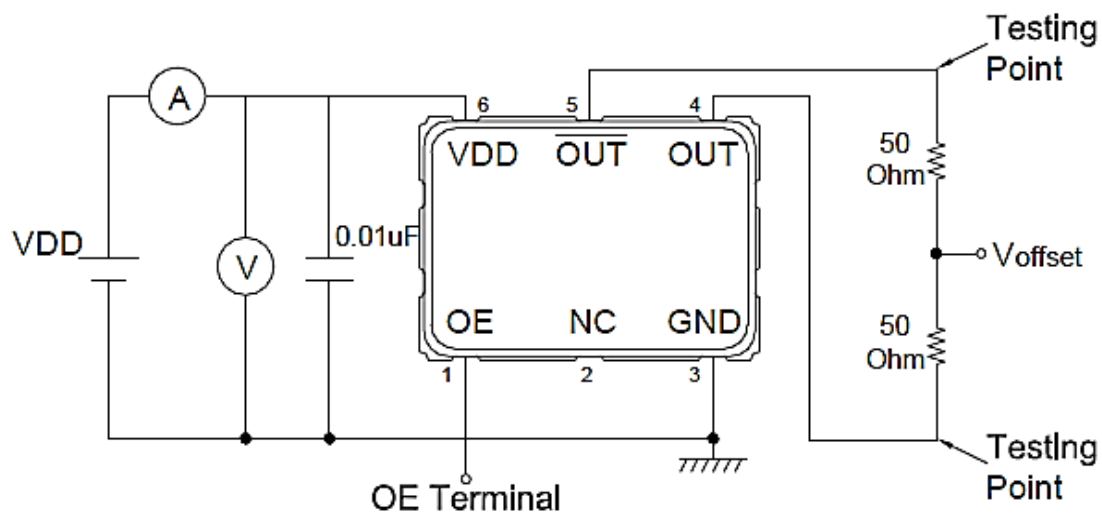
Note 1 : Inclusive of frequency tolerance at 25°C, variation over temperature , supply voltage variation , 10 years aging and vibration.

Note 2 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.

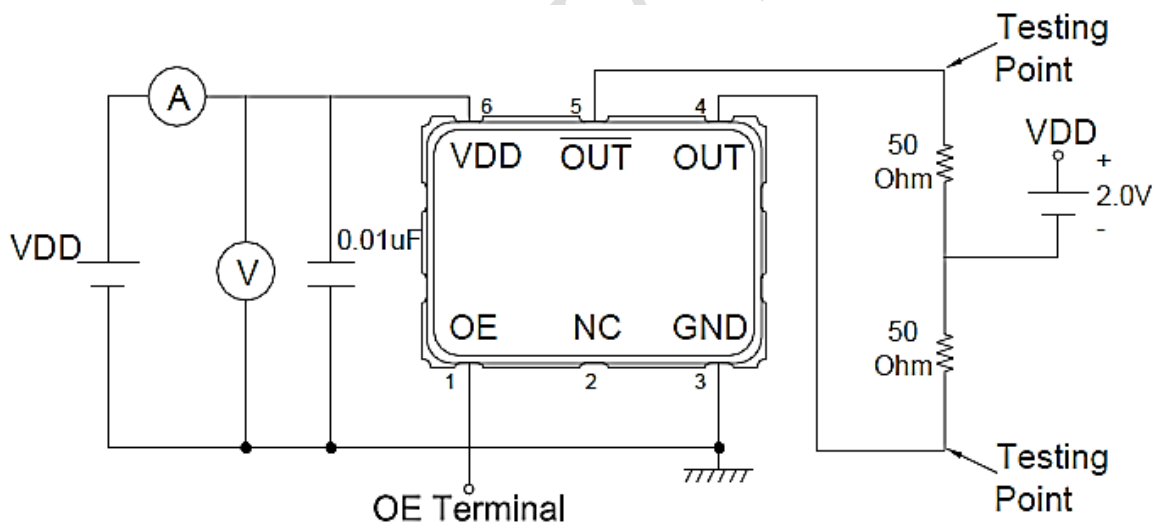
Note 3 : Phase Jitter will be slightly different according to output frequency and supply voltage.



1.2 TEST CIRCUIT(LVDS LOAD)

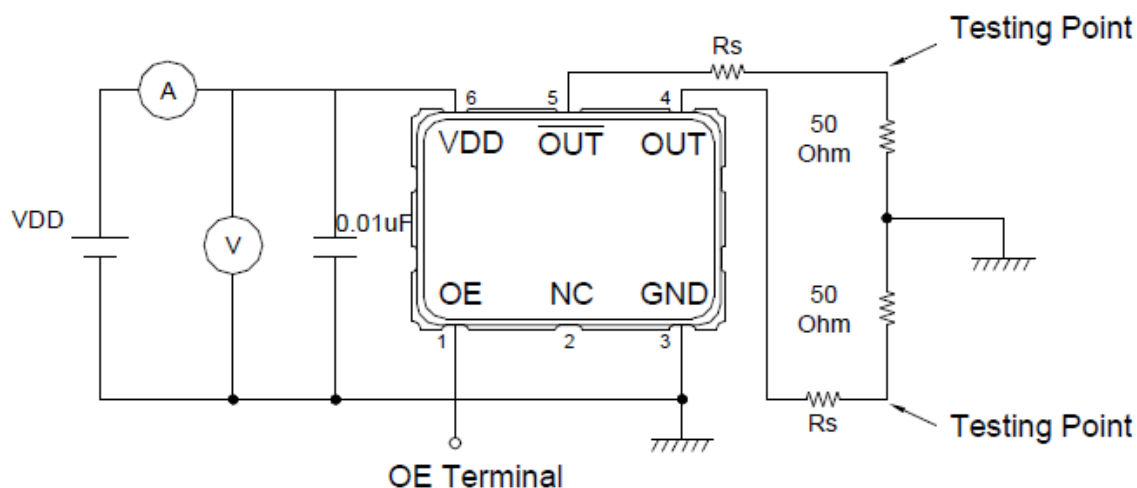


1.3 TEST CIRCUIT(LCPECL LOAD)





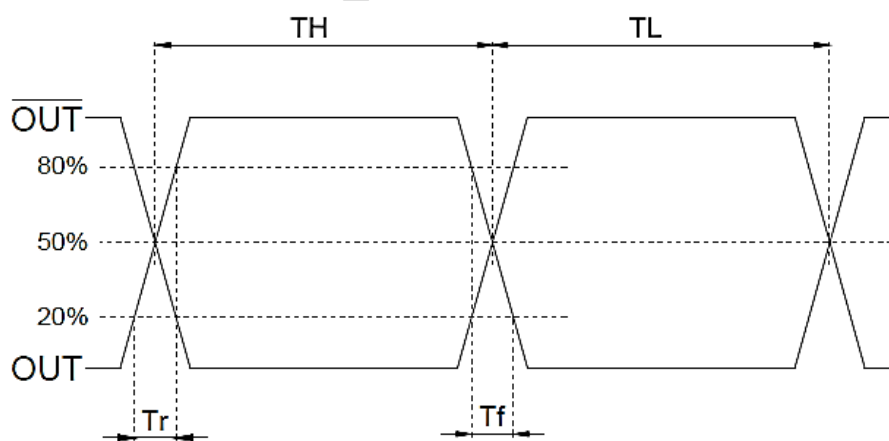
1.3 TEST CIRCUIT(HCSL LOAD)



Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All the testing equipment are 50 Ohm terminal.
3. OE terminal is open connection except OE function test.

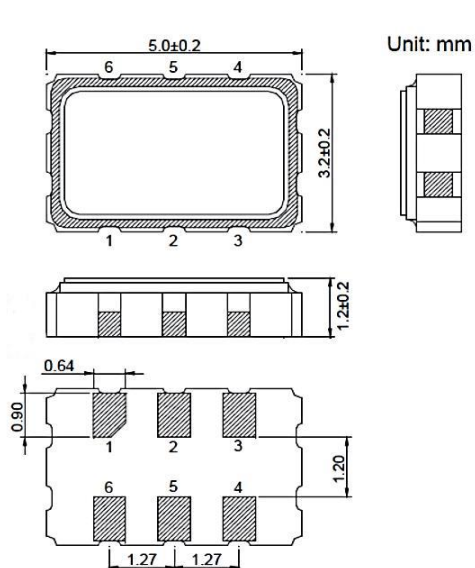
1.4 OUTPUT WAVFORM





2. PRODUCT SIZE

2.1 Dimension (Unit: mm)

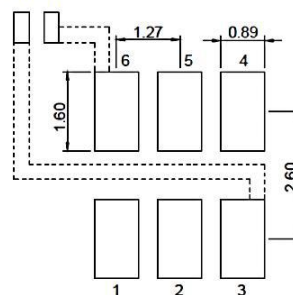


※ Pad dimension tolerance ±0.2 mm

Pin Function:

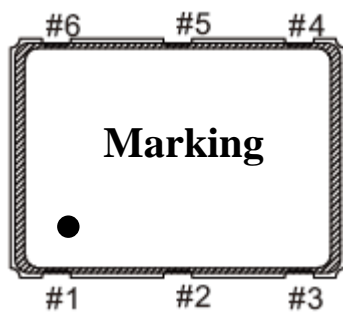
1. OE
2. NC
3. GND
4. OUT
5. $\overline{\text{OUT}}$
6. VDD

Land Pattern:



※ Power Supply Decoupling Capacitor is Required.

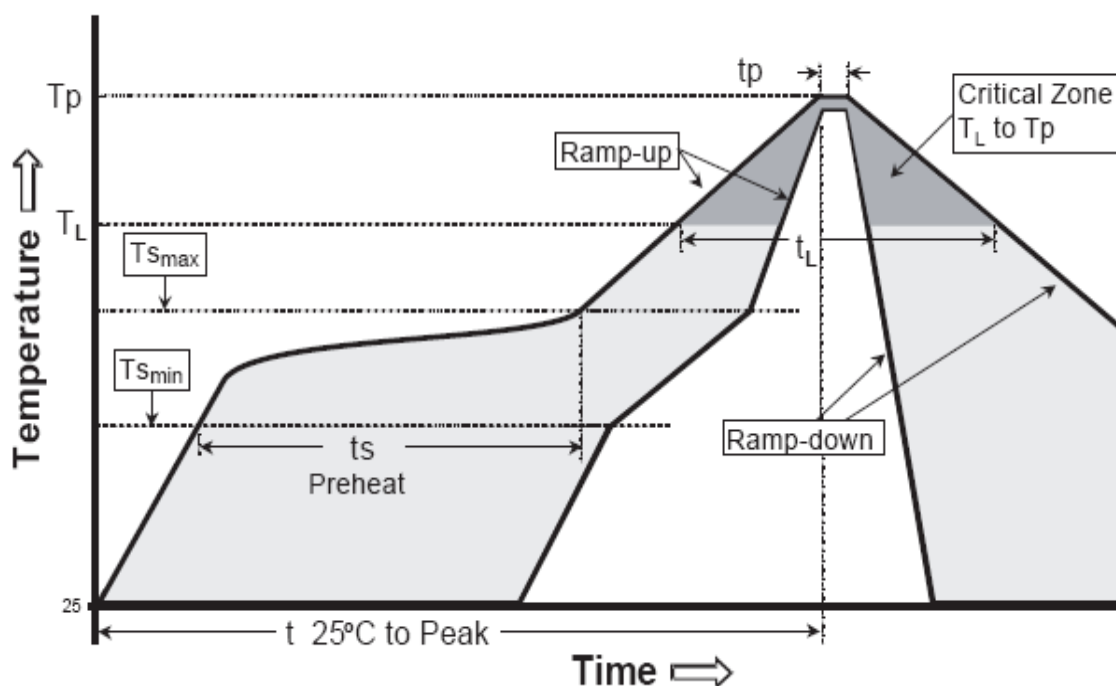
2.2 Marking





3. REFLOW PROFILES

| Profiles Feature | Pb-Free Assembly |
|---|----------------------------------|
| Average Ramp-up Rate (Ts max to Tp) | 3°C/second max. |
| Preheat <ul style="list-style-type: none"> ■ Temperature Min (Ts min) ■ Temperature Max (Ts max) ■ Time (ts min to ts max) | 125°C 200°C 60~180 seconds |
| Time maintained above <ul style="list-style-type: none"> ■ Temperature (TL) ■ Time (tL) | 217°C 60~150 seconds |
| Peak/Classification Temperature (Tp) | 260°C |
| Time within 5°C of actual Peak Temperature (tp) | 10 seconds Max |
| Ramp-down rate | 6°C/second max. |
| Time 25°C to Peak Temperature | 8 minutes max. |
| Suggest reflow times | 3 Times max |

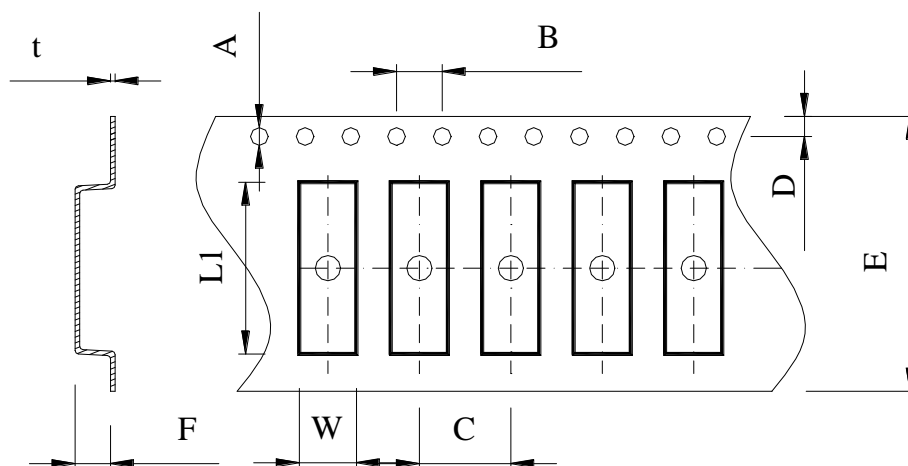


Remark: To reference JEDEC J-STD-020C



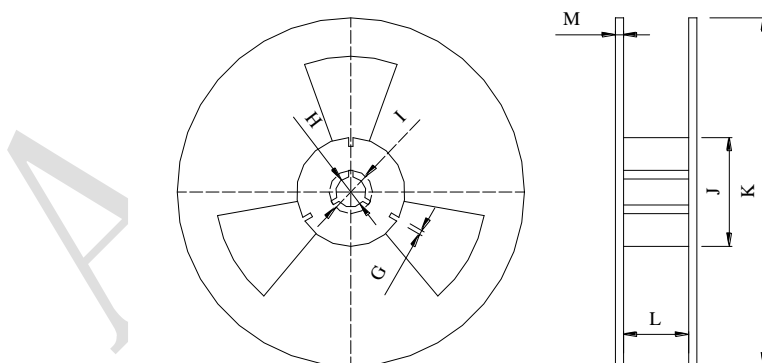
4. PACKING

4.1 Packing Method Sketch Map (Unit: mm)



| A | B | C | D | E | F | L1 | W | t |
|----------|---------|---------|----------|----------|---------|---------|---------|----------|
| 1.50±0.1 | 4.0±0.1 | 4.0±0.1 | 1.75±0.1 | 16.0±0.2 | 1.6±0.1 | 5.4±0.1 | 3.4±0.1 | 0.3±0.05 |

4.2 Reel Dimensions (Unit: mm)



| G | H | I | J | K | L | M |
|-----|------|------|------|-----|------|-----|
| 2.5 | 13.5 | 21.6 | 60.0 | 180 | 16.5 | 1.6 |

*1000pcs/Reel